SAI CHANDRAHAAS VADALI

LinkedIn | Portfolio | Personal Blog | Mobile #: +1 (650)-283-9727 | Email: scvadali@gmail.com

EDUCATION

Stanford University
M.S. in Materials Science and Engineering
GPA: 3.97/4.00
Teaching Assistant EE222: Applied Quantum Mechanics 1

Indian Institute of Technology, Madras
B. Tech, Metallurgical and Materials Engg.
GPA: 8.72/10.00
Minor: Semiconductor Devices

COURSEWORK AND LEARNING OUTCOMES

Device Physics: Power Semiconductor Devices, Special Topics in WBG Materials and Devices, Physics of Materials, Compact Modeling of Devices in ICs, Solar Cells and Device Physics
Nano Fabrication: Advanced IC Technology, IC Fabrication Lab, Electronics and Photonics Materials and Devices Lab, CVD and Epitaxy for ICs, Photonics, and MEMS
Circuit Design: Semiconductor Memory Devices and Circuit Design, Emerging Non-Volatile Memory Devices and Circuit Design, Digital Systems: From Logic gates to Processors, Analog Circuits
Specialization in Power Electronics: Introduction to Power Electronics, Converter Circuits, Converter Control, Magnetics for Power Electronics

WORK EXPERIENCE

Intel – Device Performance Group — **Portland, OR**
Device Engineer — **May '21 – Present**

Silicon Performance

- Leading performance optimization efforts in source/drain epitaxy and gate-spacer loop in the logic FEOL[1] of GAA-FET[2] architecture
- Built statistical transistor performance models on JMP for interpreting experimental signals resulting from recipe changes
- Achieved significant improvement over quarterly targets in low-voltage drive by addressing bottlenecks in DIBL[3] reduction and channel mobility, and extensive decrease in parasitic capacitance by guiding exploratory spacer deposition projects
- Received Departmental Award for leading a task force in resolving a critical epi-growth challenge in PMOS devices, mitigating severe yield and performance degradation
- Driving experimental BEOL[1] projects enhancing via-to-metal shorting margin and improving interconnect RC performance in metal pitches beyond EUV[8] scaling

Tape-out Experience

- Designed and taped out various transistor and isolation test structures to extract process margins for FEOL and BEOL, evaluating layout impact on performance

GlobalFoundries - Advanced Silicon Packaging — **Malta, NY**
Electrical Modeling and Antenna Design Intern — **Jun '20 – Aug '20**

- Optimized geometrical parameters of an aperture-coupled antenna for 5G Antenna-in-Package to maximize gain and bandwidth at 28 GHz on ANSYS HFSS[4]
- Developed RLC model of deep trench decoupling capacitors on GF[5]'s 32 nm node using KLayout and ANSYS Q3D
- Characterized insertion loss induced by 100µ Through-Silicon-Via in test vehicle for 2.5 D/psuedo-3D packaging on ANSYS HFSS and KLayout

is it fresh GmbH — **Aachen, Germany**
Antenna Engineering Intern — **Jun '18 – Aug '18**
Bachelor's Thesis* | Guide: Dr. Jan Schnitker — **Jan '19 – May '19**

- Enhanced NFC[6] reading range for ERDF[7]'s Packsense project, monitoring food freshness via printed sensors and NFC coils through experimental work

---

[1] Front End of Line/Back End of Line
[2] Gate-All-Around Field Effect Transistor
[3] Drain Induced Barrier Lowering
[4] High Frequency Structure Simulator
[5] GlobalFoundries
*Bachelor's thesis was co-advised
[6] European Regional Developmental Fund
[7] Near-Field Communication
[8] Extreme Ultraviolet
[9] Polyethylene Terephthalate
[10] Multi-level cell
[11] Very High/Ulra High Frequency

- Designed and fabricated various printed antenna configurations that led to boost in NFC read-out distance by 200% for NFC ISO14443 standards
- Achieved a sixfold reduction in bulk production costs through innovative designs of high-resistance 50 nm Aluminum on PET[9] NFC tags

PROJECTS

Semi-empirical modeling of impact ionization in wide bandgap systems
Stanford, CA
Master's Thesis | Guide: Prof. Srabanti Chowdhury **Sep '20 - May '21**

- Identified discrepancies in voltage-dependent extraction of impact ionization coefficient α in synthetic diamond diodes in experimental literature employing photomultiplication techniques on various device architectures
- Proposed a semi-empirical model for α by fitting experimental data to a harmonic sum incorporating applied electric field, electron momentum changes from E-k diagram during collisions, and electron-phonon interactions

Partial RESET-based WRITE strategies for MLC[10] in Phase-Change Memories
Stanford, CA
EE309A/B: Semiconductor memory devices and circuit design **Sep '20 – Mar '21**

- Developed a novel multi-step WRITE strategy for MLC in GeSeTe-based PCMs to minimize energy-delay product
- Awarded Best Project Award sponsored by Apple in an advanced graduate class of over 40 students for demonstrating faster, energy-efficient MLC capability with significant potential for memory-intensive AI applications
- Determined optimal number of steps and step sizes for achieving the desired resistance (bit) by analyzing the thermodynamics (energy) and crystallization kinetics (latency) of phase changes in GeSeTe
- Simulated this WRITE strategy on a specific array size using NVSim/DESTINY, with experimental results matching energy-delay product to inherently faster but less area-efficient single-bit PCM cells

Design and fabrication of printed antennas in VHF[11] and UHF[11] range
Chennai, India
Bachelor's Thesis* | Guide: Prof. Parasuraman Swaminathan **Aug '18 – Jan '19**
Flexible printed electronics

- Designed co-planar waveguide-fed antennas for GPS (1.575 GHz) and Wi-Fi (2.4 GHz) applications, using silver nanowire-based ink on FR-4 and thin PET substrates, achieving high gain with minimal return loss
- Developed a flexible, transparent capacitive touch pad using silver nanowire-based ink that demonstrated 30 Ω/sq and a transmittance of 94% at 550 nm
- Published the results of this work in - Nair, N. M., Daniel, K., Vadali, S. C., Ray, D., & Swaminathan, P. (2019). Direct writing of silver nanowire-based ink for flexible transparent capacitive touch pad. *Flexible and Printed Electronics*, *4*(4), 045001. https://doi.org/10.1088/2058-8585/ab4b04

Many-in-one wearable virtual musical instruments (Patent)
Chennai, India
Indian Patent no. 481647 **- Center For Innovation, IIT Madras** **Aug '16 – Jan '17**

- Patented gesture-controlled musical instruments with sensor-loaded gloves, eliminating the need for physical structures
- Trained classification models to interpret hand and head movements and perform diverse instruments like violin, flute, tabla, guitar, on a single pair of gloves
- Performed live at the techno-cultural show Envisage, part of IIT Madras' Shaastra[12], which had a footfall of 4000+

Indoor Positioning System using Wi-Fi
Chennai, India
Electronics Club - Center For Innovation, IIT Madras **Mar '16 – Oct '16**

- Engineered an indoor positioning system using the $5 WiFi-enabled ESP8266-01 IoT[13] module, achieving 1-2 m accuracy
- Achieved a 10x cost reduction, 3x form factor reduction versus existing solutions, prompting interest from TVS Motor Company for warehouse inventory tracking implementation
- Built a self-localizing robot mapping Wi-Fi nodes in a room using a projections onto convex sets-based trilateration algorithm while representing IIT Madras in the 5th Inter-IIT Tech Meet[14]

---

[12] Annual Technical Festival
[13] Internet-of-Things
[14] Intercollegiate Tech Competitions
[15] Proportional–integral–derivative
[16] Tech for sustainability

AWARDS

Division Departmental Award — Portland, OR
Logic Technology Development, Intel — Mar '16 – Oct '16

- Received recognition for exceptional contributions towards achieving strategic objectives within Intel's R&D organization of over 10,000 engineers

K. C. Mahindra Scholarship for Graduate Studies Abroad — Mumbai, India
Scholarship — Jul '19

- Selected from a pool of 1500+ applicants for a $6,000 scholarship by K. C. Mahindra Education Trust to support pursuing a Master's degree abroad

DAAD-University Grants Commission (UGC) Scholarship — Aachen, Germany
Scholarship — May '18

- Awarded scholarship through the DAAD-UGC program, facilitating a fully funded summer internship at Julich Research Center

Asia and India book of record holder — Chennai, India
Center For Innovation, IIT Madras — Oct '17

- Set the record for the ``Most robots (45) simultaneously cleaning a badminton court" while mentoring 270+ undergraduate and graduate students
- Prominent media coverage – TV coverage, print media

Mudiraj Scholarship — Hyderabad, India
Complete Tuition Support, Johnson Grammar School — 2005-2012

- Granted full tuition coverage for exceptional academic performance from primary through high school

LEADERSHIP & MENTORSHIP ROLES

Teaching Assistant — Stanford, CA
EE222: Applied Quantum Mechanics 1 by Prof. David Miller — Fall 2020

- Instructed in office hours, clarified complex concepts and problem sets for a class of 50 graduate students
- Rated as "Extremely Effective" in instruction quality and clarity by over 60% students

Head, Electronics Club — Chennai, India
Center For Innovation, IIT Madras — 2017-2018

- Led a team of 6 coordinators and conducted 10+ sessions on diverse topics ranging from soldering, PID[15] controller design, IoT, analog and digital circuits, etc.
- Mentored student projects in impactful areas like unmanned robotics, rural smart lighting, personalized medical monitors, and more
- Planned and executed an event for autonomous crowd-control technologies for the 6th edition of Inter-IIT Tech Meet

Head, Extra-Mural Lectures — Chennai, India
IIT Madras — 2017-2018

- Led a team of 20 students and conducted 19 lectures on diverse topics ranging from contemporary global economic issues, social entrepreneurship, wildlife and habitat conservation, indigenous defense technologies, music and vernacular lyric-writing

HOBBIES

- Running – HM PR 1:28:34 @ Portland Marathon 2023
- Biking, bikepacking – adventures across Switzerland, biking from Bordeaux to Basque country
- Carnatic Singing

COMMUNITY ENGAGEMENT

- Mentored 100+ incoming freshmen via one-on-one sessions to deal with emotional, social, academic stressors
- Technical advisor for the Carbon Zero Challenge[16] winner, "Intelligent Lighting system," addressing power wastage in rural Indian lighting."